REMARKS

Claim 13 is amended. Claims 29-36 are added. No new matter is added as the new claims are supported by the originally-filed application at pages 7-10 of the specification and Figs. 5-6. Claims 1-20 and 29-36 are pending in the application.

Claims 1-20 stand rejected under 35 USC §103(a) as being unpatentable over Ku et al. ("The Application of Ion-Beam Mixing, Doped Silicide, and Rapid Thermal Processing to Self-Aligned Silicide Technology", VLSI Technology, Systems and Applications, May 17-19, 1989, pages 337-341). Applicant disagrees and requests reconsideration.

Claim 1 recites forming a silicide layer against a polysilicon layer and providing a conductivity-enhancing impurity within the silicide layer. Ku is completely devoid of teaching or suggesting such a limitation as recited in claim 1. Ku teaches forming a silicide over an Si wafer and implanting impurity ions into the silicide as a source for subsequent formation of source/drain regions by annealing the wafer to drive the ions from the silicide into the Si wafer (col. 1, paragraphs 2-4 of pg. 340 for p^+ region formation; col. 2, last paragraph of pg. 340 for n^+ region formation; Fig. 1 showing the n^+ region). Fig. 1 of Ku clearly labels a $TiSi_2$ layer **only** over the Si wafer above a region to be sequently processed into the n^+ source/drain region. Accordingly, in no fair or reasonable interpretation does Ku teach or suggest forming a silicide layer against a polysilicon layer **and** providing a conductivity-enhancing impurity within the silicide layer as recited in claim 1. Ku fails to teach or suggest a positively recited limitation of

claim 1, and therefore, the obviousness rejection is inappropriate and should be withdrawn. Applicant respectfully requests allowance of claim 1 in the next Office Action.

Claims 2-12 depend from independent claim 1, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are neither shown or taught by the art of record.

Claim 13 recites a method of lowering the resistivity of a metal-silicide layer comprising doping the metal-silicide layer with phosphorous. Ku teaches doping a silicide layer with boron ions (col. 1, third paragraph of pg. 340) and arsenic ions (col. 2, last paragraph of pg. 340). Accordingly, in no fair interpretation does Ku teach or suggest doping the metal-silicide layer with phosphorous. Since Ku fails to teach a positively recited limitation of claim 13, the obviousness rejection is overcome. Applicant respectfully requests allowance of claim 13 in the next Office Action.

Claim 14 depends from independent claim 13, and therefore, is allowable for the reasons discussed above with respect to the independent claim, as well as for its own recited features which are neither shown or taught by the art of record.

Claim 15 recites forming a silicide layer against a layer of polysilicon **and** providing a conductivity-enhancing impurity within the silicide layer. For the reasons discussed above with respect to claim 1, Ku fails to teach forming the silicide layer against the layer of polysilicon **and** providing the conductivity-enhancing impurity within the silicide layer as recited in claim 15. Since Ku fails to teach a positively recited

limitation of claim 15, claim 15 is allowable as written. Applicant respectfully requests allowance of claim 15 in the next Office Action.

Claims 16-19 depend from independent claim 15, and therefore, are allowable for the reasons stated above regarding the independent claim, as well as for their own recited features which are neither shown or taught by the art of record.

Claim 20 recites forming a silicide layer against a layer of polysilicon and providing a conductivity-enhancing impurity within the silicide layer. For the reasons discussed above with respect to claim 1, Ku fails to teach forming the silicide layer against the layer of polysilicon **and** providing the conductivity-enhancing impurity within the silicide layer as recited in claim 20. Ku fails to teach a positively recited limitation of claim 20, and for at least this reason, claim 20 is allowable as written. Applicant respectfully requests allowance of claim 20 in the next Office Action.

Moreover, claim 20 recites subjecting the silicide layer to a processing step of over 850° C for at least 10 seconds while exposing the silicide layer to an oxygen-comprising atmosphere. Ku teaches exposing silicide layers to nitrogen (col. 1, paragraph 3 of pg. 340; col. 1, paragraph 4 of pg. 340; col. 2, last paragraph of pg. 340). Accordingly, in no fair or reasonable interpretation does Ku teach or suggest subjecting the silicide layer to a processing step of over 850° C for at least 10 seconds while exposing the silicide layer to an oxygen-comprising atmosphere as recited in claim 20. Ku fails to teach a second positively recited limitation of claim 20. For this

additional reason, claim 20 is allowable as written. Applicant respectfully requests allowance of claim 20 in the next Office Action.

Further, Applicant herewith submits a duplicate copy of the Information Disclosure Statement and Form PTO-1449 filed together with this application on June 11, 1999. No initialed copy of the PTO-1449 has been received back from the Examiner. To the extent that the submitted references listed on the Form PTO-1449 have not already been considered, and the Form PTO-1449 has not been initialed with a copy being returned to Applicant, such examination and initialing is requested at this time, as well as return of a copy of the initialed Form PTO-1449 to the undersigned.

This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 3-13-02

By: _____

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/332,271
Filing Date ..... June 11, 1999
Inventor ..... Klaus Florian Schuegraf et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 2812
Examiner ..... Ron E. Pompey
Attorney's Docket No. MI22-532
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects, and Wordline, Transistor Gate, and Conductive Interconnect Structures

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO DECEMBER 21, 2001 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

13. (Amended) A method of lowering the resistivity of a metal-silicide layer comprising doping the metal-silicide layer with ~~a Group III dopant or a Group V dopant~~ phosphorous.

Please add the following new claims:

29. (New) A method of forming a conductive line comprising:

forming a polysilicon layer;

forming a silicide layer over and proximately adjacent only the polysilicon layer; and

providing a conductivity-enhancing impurity within the silicide layer.

30. (New) The method of claim 29 further comprising exposing the silicide layer to an oxygen-comprising atmosphere.

31. (New) The method of claim 29 wherein the conductivity-enhancing impurity comprises phosphorous.

32. (New) The method of claim 29 further comprising providing a dopant within the polysilicon layer to a concentration of at least about 1×10^{19} ions/cm^3.

33. (New) A method of forming a conductive line comprising:

providing a substrate;

forming a polysilicon layer over the substrate;

forming a silicide layer over the polysilicon layer and substrate; and

after the forming of the silicide, patterning the polysilicon and silicide layers to form a conductive line.

34. (New) The method of claim 33 further comprising providing a conductivity-enhancing impurity within the silicide layer.

35. (New) The method of claim 34 wherein the providing of the conductivity-enhancing impurity is performed after the patterning of the polysilicon and silicide layers.

36. (New) The method of claim 34 wherein the providing of the conductivity-enhancing impurity is performed before the patterning of the polysilicon and silicide layers.

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